Low Voltage Analog CMOS Design

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Abstract

The purpose of this paper is to survey the subject of low voltage design rather than to focus on a specific problem. The paper accomplishes this by outlining some of the difficulties facing Low Voltage Analog CMOS designers as presented by the *Low-Voltage Low-Power Analog CMOS* conference held April 20—24 in Montery, California sponsored by Mead Microelectronics, Inc. The review includes inherent limitations in CMOS design, architectural trends, and a brief overview of BiCMOS. There is also a focus on data converters and some of their analog building blocks.

Contents

I. Introduction

This paper is largely based on the proceedings of the Low Voltage, Low Power Analog CMOS conference held on April 20-24, 1998 in Monterey CA.

Analog Low Voltage design is becoming increasingly important as process technologies shrink, and supply voltages shrink with them. Many ASICs (Application Specific Integrated Circuits) contain mixed signal content (both analog and digital circuits), almost always in the proportion of big digital to small analog. This is true for other types of IC's as well. Process technology is primarily driven by the needs of digital circuits over analog circuits. The following equation relates voltage and operating frequency to system power (P):

$$P = CV^2 f$$ [1]

C represents the gate capacitance of MOS devices. As frequencies (*f*) continually scale upwards, heat production becomes a major problem because of high component density. The most effective way to lower power is to decrease the operating voltage (V).

Many processes often add extra steps to support analog circuits running at higher voltages than their digital counterparts, increasing the cost of the chip. Chips that have separate analog and digital voltage supplies are common, but this adds to the total system cost. The goals of analog designers must be to lower the voltage requirements of their circuits, thus lowering system cost.

Over the years, many traditional analog system blocks such as filters have been moved to the digital realm to save cost and increase yields. With digital circuitry driving most processes, the tolerances of transistors and on-chip passive devices (resistors and capacitors) are poor. Since digital yields are less sensitive to these tolerances, it is economically viable to convert as much analog circuitry into digital as possible. Therefore converters are moving closer and closer to the input signals, and other functions such as filters are being moved from the analog domain to the digital domain.

II. Technological Limitations

Reducing power dissipation by scaling device sizes and power supplies is much more effective for digital circuitry than analog. Digital circuits do not dissipate power when they are not switching, but analog circuits do. All analog circuits contain sections that need to be biased with a DC current, so there is always current flowing. Low voltage limitations of analog circuits are also dependent on the threshold voltage of MOS transistors. Supply voltages are dropping whereas the threshold voltages of MOS transistors have not been scaling similarly [11], and this limits our ability to stack of transistors [2]. Another problem occurs in switched capacitor circuits. A reduction in supply voltage limits the voltage swing of signals, since the use of analog switches requires at least a V_T in voltage drop to ensure the switch is on. Charge injection also becomes a larger error factor at these voltages. With the drop in voltage, it is also more difficult to generate precise currents because of a lack of sufficient headroom, resulting in noisier currents [3].

The two major problems with device scaling are hot-carrier effects and the possibility of oxide breakdown. Hot-carriers have a higher energy than the thermal energy. As devices get

smaller, the reverse bias drain to substrate junction can have a very high electric field. Some carriers may get injected into the depletion layer, and with the high electric field, they may gain enough energy to cause impact ionization [13]. This can lead to other problems such as electrons tunneling into the gate oxide, modifying the behavior of the transistor. Structures such as lightly-doped drains have been created to lower this electric field. Breakdown of the oxide occurs when the gate insulation can no longer support the electric field imposed upon it by the gate voltage, resulting in a gate to body short. The thinner the gate oxide is, the larger the resulting electric field.

III. MOS designs vs. BJT design

The following table outlines major differences between MOSFET (Metal Oxide Semiconductor Field Effect Transistor) and BJT (Bipolar Junction Transistors) [4]:

Figure of merit	**MOS**	**BJT**
DC current control	No	Yes
Current Noise	Low	High
LF noise	High	Low
Voltage Switch	Yes	No
Current matching	Poor	Good
Voltage offset	Large	Small
Control of temperature effects	Bad	Good
Low voltage f_T	Low	High
Low voltage max current	Small	Large
Control voltage swing	Large	Small
Quadratic Characteristic	Yes	No
Low power logic	Yes	No

Table 1: MOS versus BJT characteristics

The most important differences are the superiority of the BJT for Low voltage, a higher f_T and its larger maximum current versus the MOSFET's. The former is important because the digital world is moving towards lower voltage for the purpose of gaining speed through lowered power dissipation. The following diagram shows how a BJT can be created using a purely CMOS process:

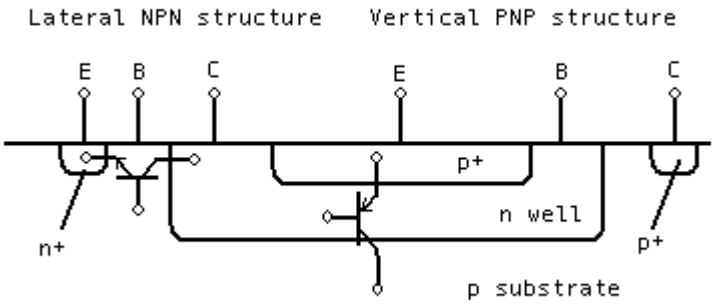


Figure 1: Bipolar transistors in a CMOS process

These types of transistors have limited use since they have poor Betas (gains); they are actually parasitic devices. The vertical PNP is the most commonly used type of BJT, normally relegated to bandgap circuits where a high Beta is not necessary. The NPN version is generally not used since the base would need to be connected to a positive voltage (likely V_{DD}) to be used as in diode in a bandgap. This is unacceptable since the substrate is (and must be) tied to V_{SS}. For these reasons BJT in a strictly CMOS process cannot be used to take advantage of the positive figures of merit outlined in table 1.

In a BiCMOS process, one can build good bipolar transistors as well as good CMOS transistors. As usual, there is a trade off in that it is sometimes prohibitively expensive (about 50% more than standard CMOS [7]) to use in applications where there is a large digital section and a small analog section. CMOS dominates because production volume dictates the process to be used. CMOS has come such a long way in terms of speed that it is no longer inferior. Below is a cross-section of a BiCMOS process:

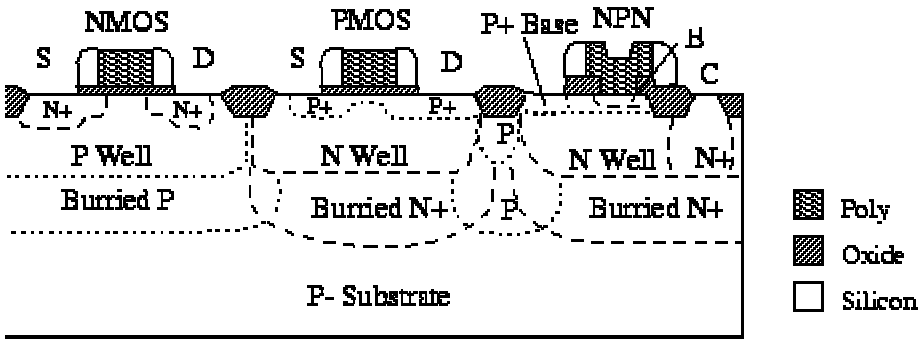


Figure 2: BiCMOS cross-section [7]

The advantages of being able to build good BJTs are evident in circuits such as op-amps, comparators, and sample and hold circuits. For opamps and comparators, advantages over equivalent CMOS devices include speed (by increasing the unity-gain frequency), greater resistive drive strength [8], and lower offsets voltage (in CMOS large devices must be used to minimize input offset). Finally since good diodes are available in a BiCMOS process, sample and holds would be able to use diode bridge circuits [8].

Research is also progressing in operating MOSFETs in a fashion where they behave as BJTs. The benefits of this technique include 100% compatibility with the CMOS process, low 1/f noise, and low offset voltage. Since it is not a true BJT, the device suffers from a low maximum current and a low maximum speed. The diagram below illustrates how to operate a MOSFET as a BJT:

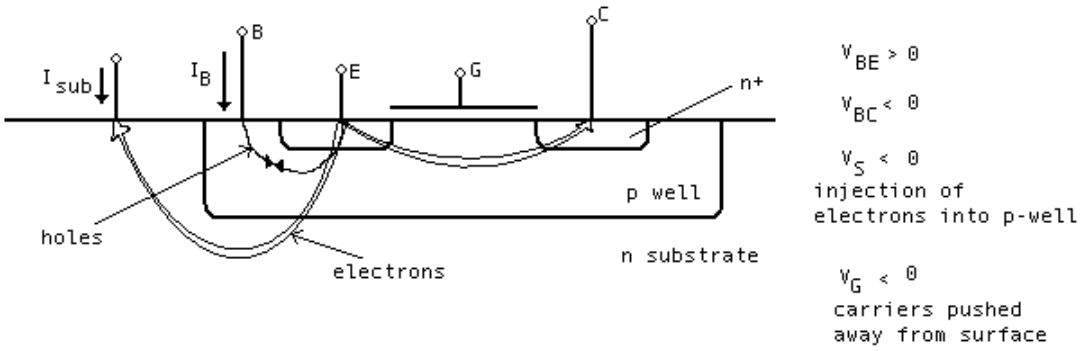


Figure 3: NMOS transistor operated as a BJT [4]

IV. Data Converters

Data converters are fundamental analog cells that will be with us for a long time. They are crucial because they provide digital systems with an analog connection to the outside world. Below is a list of both analog to digital and digital to analog converters, and their uses:

Resolution	Conversion Rate	Applications
16 bits	< 1kHz	Low frequency measurements, temperature, etc.
16 bits	50kHz	High Quality Digital Audio
15 bits	8kHz	Voice band Telecom
13 bits	200kHz	ISDN
12 bits	5MHz	Imaging, Radar
10 bits	20-50MHz	High definition Video, HDTV, Digital Video Camera, Cable TV decoder modem
6-10 bits	<50MHz	Wireless LAN
6-8 bits	>200MHz	High speed instrumentation, magnetic storage read channel
8 bits	15MHz	Video

Table 2: Analog to digital and digital to analog converter uses [5].

Analog to digital converters fall into two basic categories: Nyquist Rate and Oversampled.

Nyquist rate analog to digital converters:
Level at a time: This type of converter works by charging a capacitor to a referenced voltage and then discharging it at a rate proportional to the input voltage, and counting the clock cycles it takes to do so. This method is slow, but it can have very low offset and gain errors, and have a high resolution with high linearity. An example of this type of converter is an integrating converter such as a dual slope converter.
Bit at a time: These converters typically have one comparator that is used to compare the input signal to a voltage that is fed back from a D/A. The voltage from the D/A is generated by a previous cycle. The MSB (most significant bit) is decided first, and then the converter iterates down to the LSB (least significant bit), playing a guessing game. The droop in the sample and hold (S & H) circuit and offset in the comparator must be minimized. Examples of this include successive approximation and cyclic (algorithmic) converters. The following is a simplified block diagram:

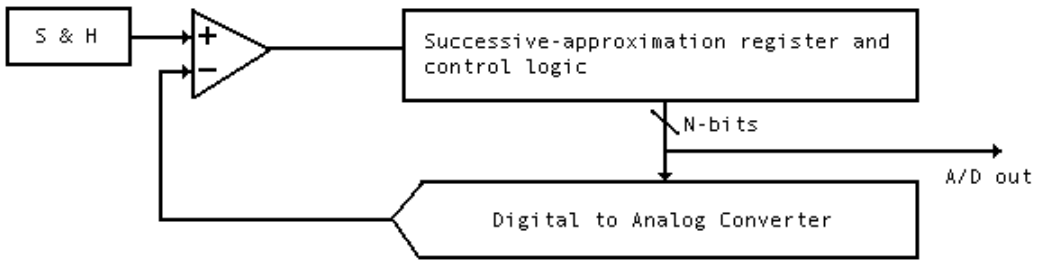


Figure 4: Successive approximation A/D

Word at a time: These are more commonly called flash converters or parallel comparators because they perform an entire conversion in one clock cycle. These types are the fastest, but have limited resolution. They work by breaking down the reference voltage into discrete steps, comparing those voltages to the input voltage to determine the magnitude of the input. These converters double in size with every bit of resolution added since you need 2^{N-1} converters (one for each discrete step in the reference voltage divider).
Multibit at a time: These converters convert more than one bit during one clock cycle. This category includes two step A/Ds and pipelined A/Ds. The advantages of these converters stem from being a hybrid between bit at a time converters and word at a time converters. These converters can also be very fast since they can begin a new conversion before the previous one is complete, although this results in latency between the sample clock and the data.

Oversampling converters
Predictive: an example of this type is Delta Modulation.
Noise Shaping: Oversampling is performed by bandlimiting signals of interest limited to less than one half the sampling rate. Oversampling is measured by the oversampling ratio (OSR) which is equal to the sampling frequency divided by twice the bandlimited frequency. Delta-Sigma converters fall into this category of oversampling converters. Below is a block diagram for an oversampling A/D converter.

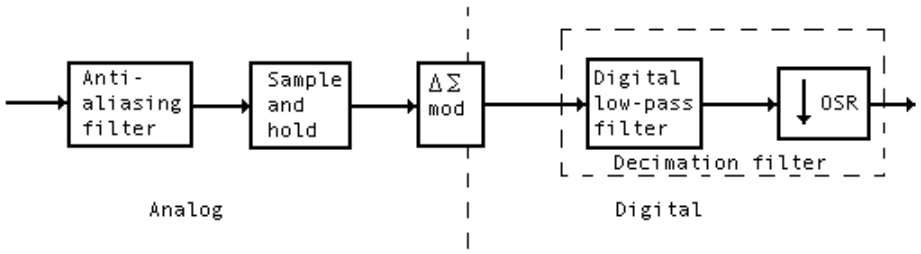


Figure 5: Block diagram for a basic oversampling A/D converter.

The first stage consists of a continuous time filter such as a gm-C, but if the OSR is large, then the filter can be as simple as a RC low-pass filter. The signal is then held by the sample and hold, and processed by the ΔΣ modulator which extracts noise shaped, low resolution digital data. If a switched capacitor analog channel is used, then the sample and hold can be avoided since sampling is inherent in a switched capacitor circuit. The last section is a decimation filter that can

be thought of as a low-pass digital filter followed by a downsampler. It effectively turns the low resolution digital signal into a high resolution digital signal.

V. Analog Building Blocks

Op-Amps & Comparators

Systems such as switched-capacitor and sample and holds rely on good MOS switches and good opamps. Opamps provide a precise summing node, therefore they need to have high gain for a precise closed loop gain. Another important spec is opamp speed (bandwidth, and settling time) because they can limit the clock frequency in switched-capacitor systems [1]. In general, low voltage analog designers use the differential mode of operation, since this can double the voltage swing, suppress even-order distortion, improve the power supply rejection, and suppress effects of charge injection [6]. The following are three sections dedicated to the common building blocks of opamps and comparators. Variations in circuit design are explored.

Current Mirrors:
Below are five types of current mirrors taken from [16], common in low voltage design:

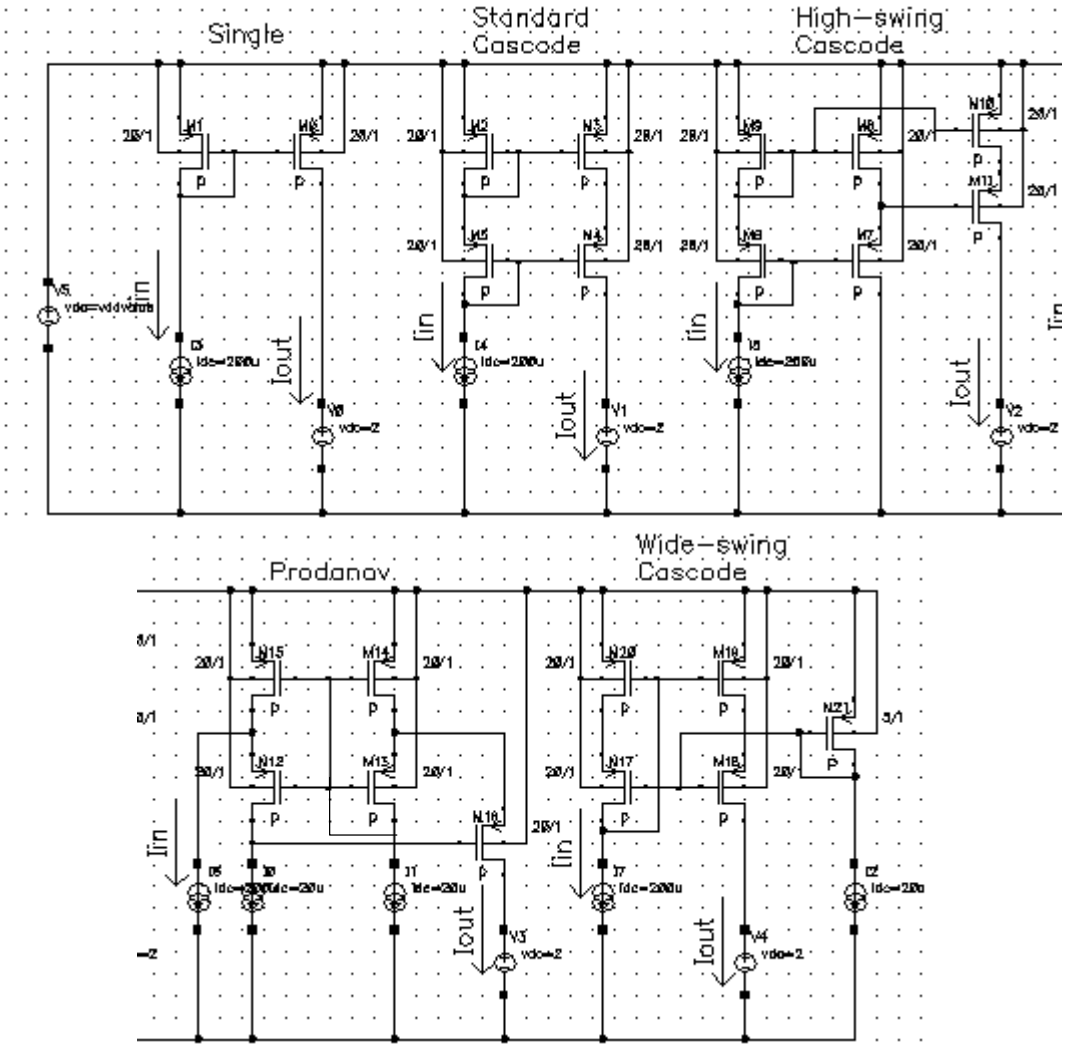


Figure 6: Different current mirror architectures.

The current mirrors used most often in analog design are the single, the wide-swing and the standard cascode. If a high impedance output is required, the most useful configuration is the aptly named wide-swing cascode. It only has an output voltage requirement of 2ΔV whereas the standard cascode has an output voltage requirement of V_T + 2ΔV. The single transistor current mirror is almost unusable unless accuracy is not an important design parameter; because of the larger V_{DS} changes, the output current is modulated to a large degree. Figure 7 shows the results from the DC simulation where the output voltage was swept from 0 to 3.3V. This tests the ability of each current mirror to source the correct amount of current to loads with varying voltage requirements. This test is especially important because current mirrors are used to bias virtually every stage of an opamp or comparator. The voltage requirement of a current mirror in an output stage affects the performance of the opamp. A common architecture for a DAC is basically a glorified current mirror. In this case, the output voltage swing and output accuracy from a current mirror is crucial. From the simulations, it seems the Prodanov (blue) current mirror (figure 7) is the best choice for very wide output voltage swings, because it maintains its output current at higher output voltages than the other current mirrors.

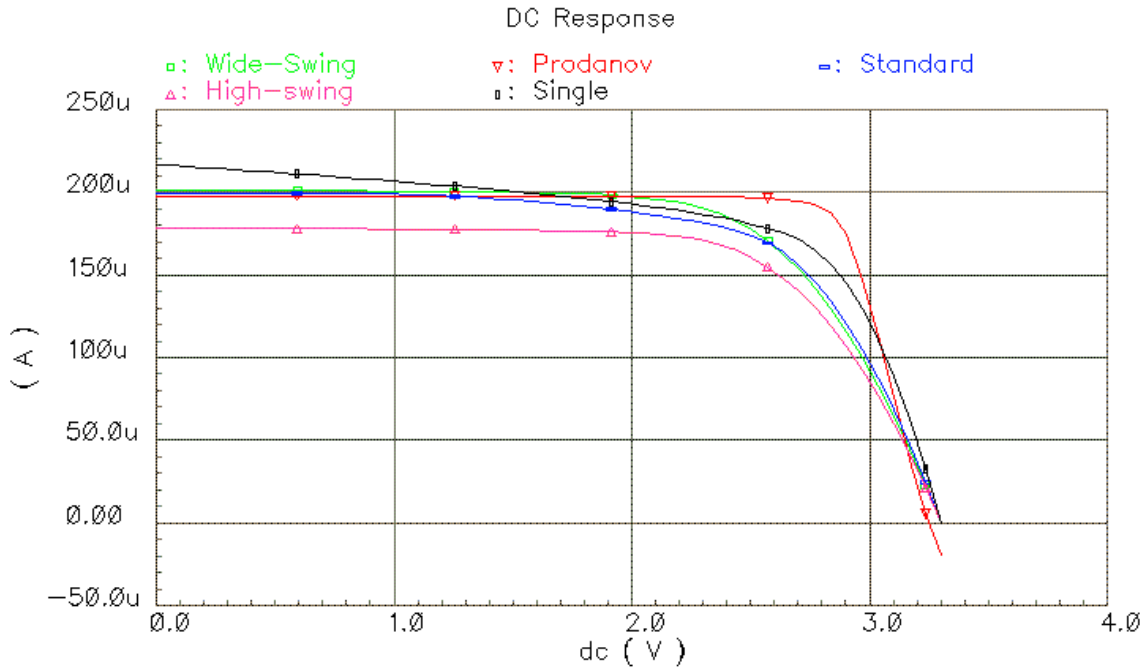


Figure 7: Current mirror DC response with varying output voltage.

DC performance is not the only important performance metric. Careful attention must also be paid to AC performance. The AC simulation results are shown in Figure 8. The Prodanov mirror is the first to deviate from 0 dB, showing it as the least adept at high frequencies. These results agree with simulation results reported in [11]. The circuit exhibits a gain at high frequencies (around 100MHz) before it attenuates.

A good choice for high frequency applications is the single transistor current mirror, however this circuit is inaccurate and has a lower output impedance than the other circuits available. The recommend current mirror is the wide-swing cascode. This current mirror has the best high frequency performance, maintaining unity gain (exactly what you want a current mirror to do) past 500 MHz. An important fact to remember with this current mirror is that the voltage biasing transistor (M21) should be one-fourth the size of all the other transistors if they are all the same size.

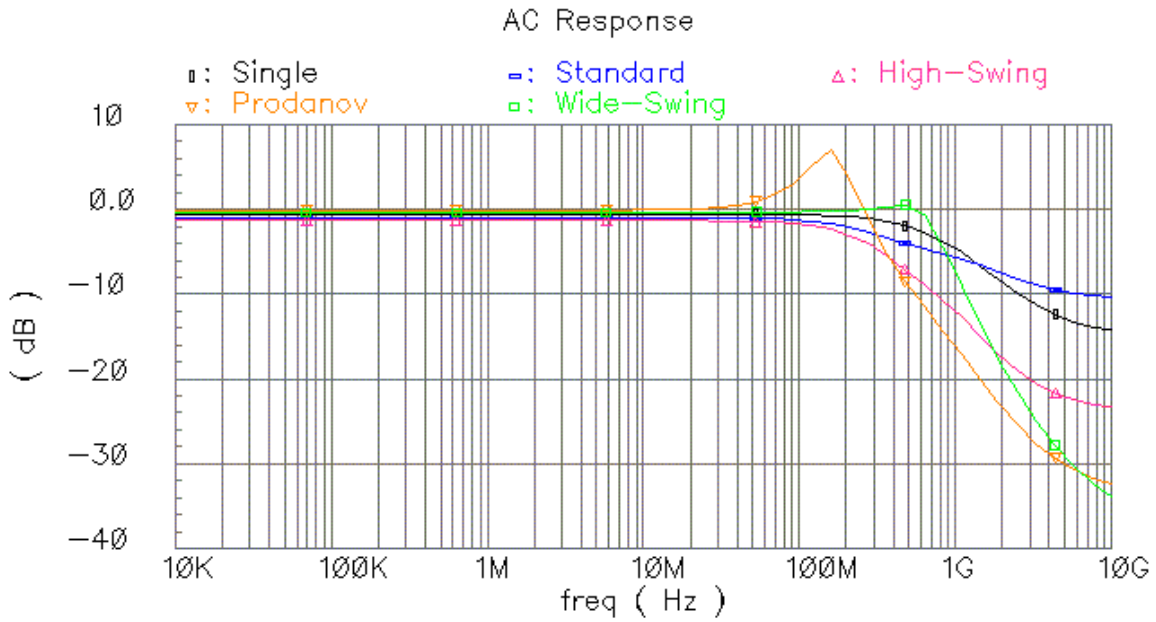
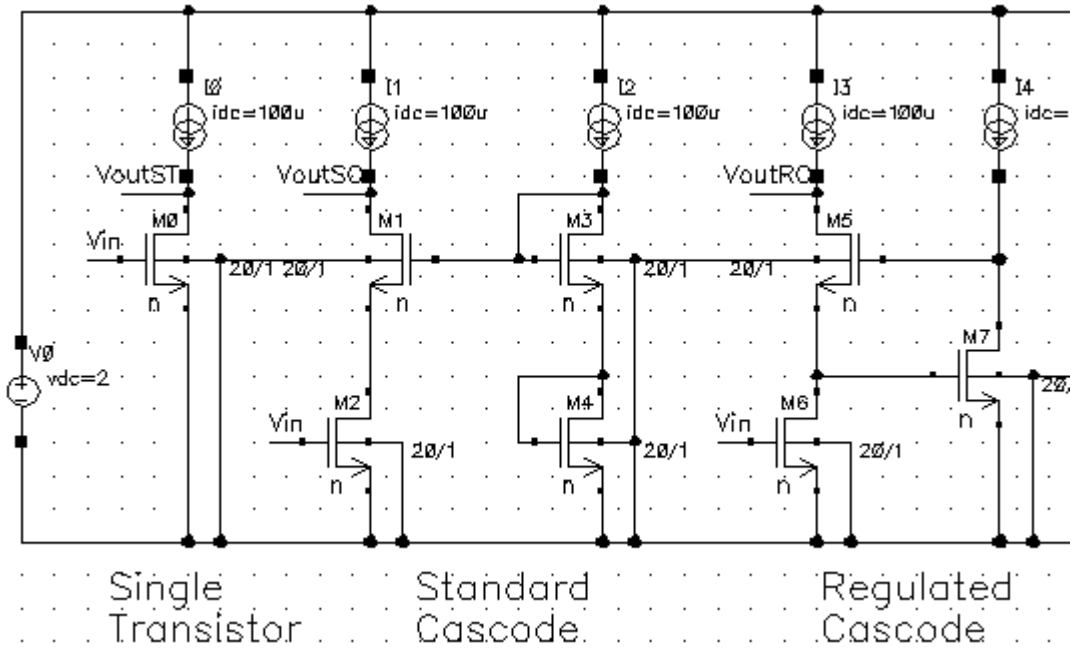


Figure 8: Current mirror AC response.

Cascode Structures:



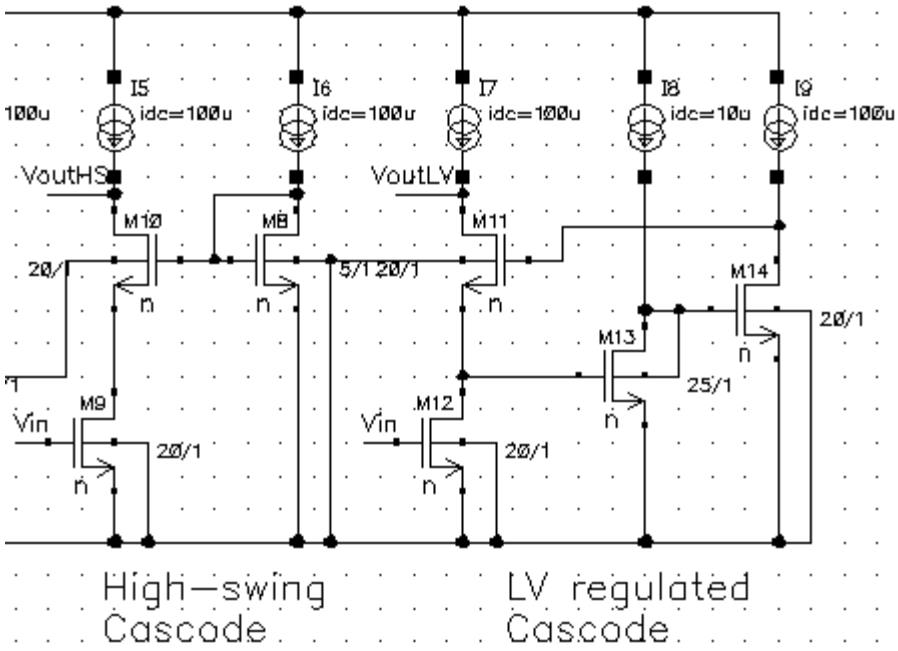


Figure 9: Different types of cascode structures.

A more appropriate name for this subsection might have been gain stages because the single transistor gain stage is also discussed. A cascode gain stage is a stage where a common source transistor is feeding into a common gate connected transistor. The voltage input is connected to the common source transistor, and the common gate transistor has its gate tied to a voltage bias. There are a few ways to connect the bias – it can be an uncontrolled bias, or a feedback configuration such as the two regulated examples can be used. In the regulated examples, a higher output impedance in realised. It is also important to note that high quality, high output impedance current mirrors must be used as the current sources to realize a high gain stage (a cascoded current mirror is usually used in this case). Below are the DC output characteristic plots:

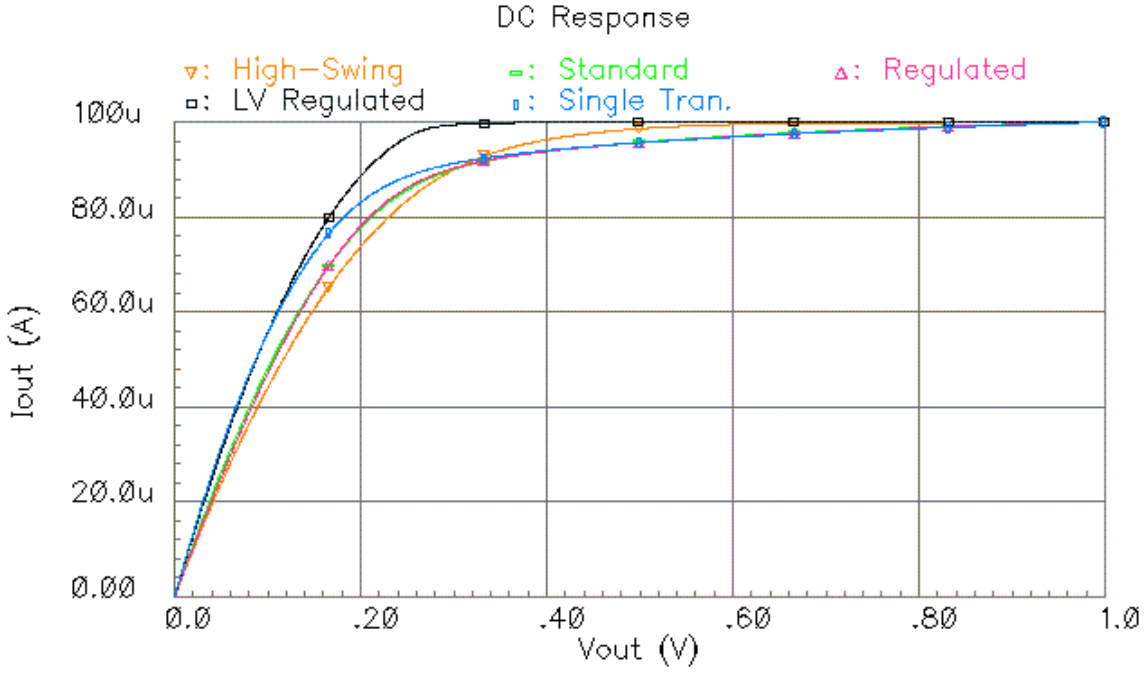


Figure 10: DC output characteristics of various cascode gain stages

The output impedance of the cascode stage can be derived by calculating the inverse of the slope of the waveform at any point. The output impedance varies as a function of output voltage. It can be seen from the simulation results that the Low Voltage Regulated cascode is the best performer at low output voltages, maintaining a high output impedance over a greater range than the rest. It also has the highest output impedance at moderate output voltages.

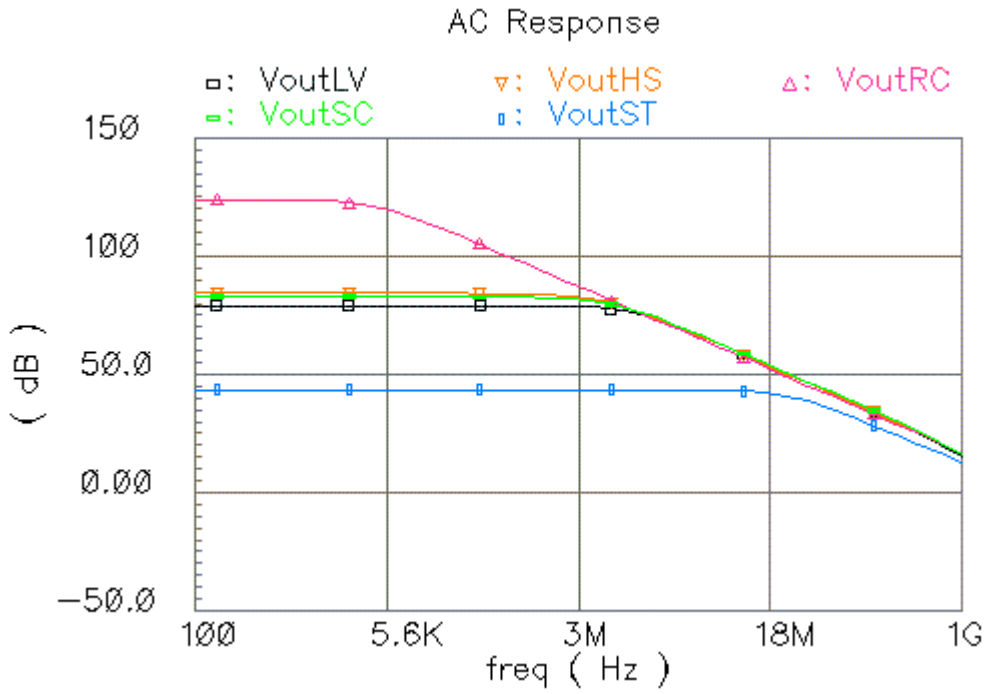


Figure 11: Cascode frequency response.

It can be see from the frequency response curves (figure 11) that the Regulated Cascode (RC) has the highest gain at DC and that the Single Transistor (ST) configuration has the lowest. This is expected, since a cascode with a feedback arrangement has a higher output impedance at low frequencies. However, these cascodes also start to roll off earlier because the feedback is slower at higher frequencies, thus decreasing the gain. An interesting note is that the roll-off and the gain bandwidth product is the same for all the types of cascode. This can be explained by the following derivation:

These calculations are accurate to a first order approximation. Assume R_{out} is the output resistance of the cascode and C is the capacitance at that node. Then the transfer function for the amplifier can be given by:

$$\frac{V_{out}}{V_{in}} = A \cdot \frac{1}{1 + sR_{out}C} = \frac{-g_m R_{out}}{1 + sR_{out}C}$$

To find the Gain Bandwidth Product we take the magnitude of the transfer function and set it equal to one and solve for the frequency:

$$1 = \frac{g_m R_{out}}{\sqrt{1 + (\omega R_{out} C)^2}} \Rightarrow 1 + (\omega R_{out} C)^2 = (g_m R_{out})^2 \Rightarrow \omega = \sqrt{\frac{1 + (g_m R_{out})^2}{(R_{out} C)^2}}$$

One can argue that "1" is small compared to the gain of the system ($g_m R_{out}$), thus R_{out} cancels from the equation and it reduces to:

$$\omega = \frac{g_m}{C}$$

Therefore the Gain Bandwidth Frequency is not related to the output impedance.

The Differential Pair:

Below are P and N differential pair configurations. The input voltage is limited by:
NMOS: $V_{SS} + V_{satn} + V_{gsn} < V_{CM} < V_{DD}$ and
PMOS: $V_{SS} < V_{CM} < V_{DD} - V_{satp} - V_{gsp}$

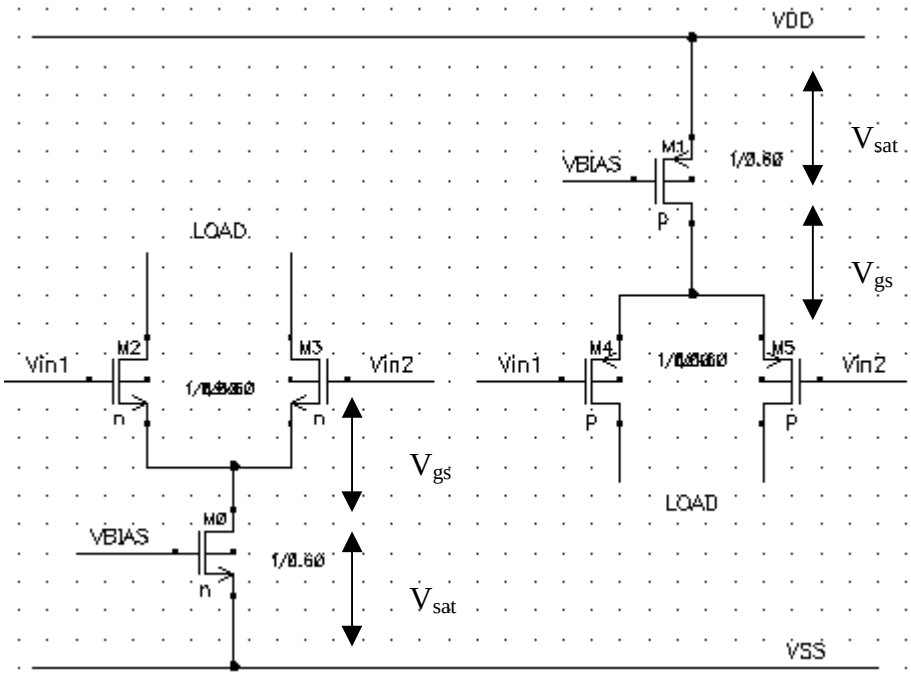


Figure 12: Classic Differential pairs with active loads.

Considering this analysis, one can conclude that classical techniques are sufficient down to a supply voltage of about 2.5V [2]. One thing we can do to solve the low voltage problem includes putting the N and P input stages in parallel for rail-to-rail operation. Unfortunately, the total g_m of the input stage wouldn't be constant as the common-mode voltage is varied (the g_m will be higher when both differential pairs are on). Therefore optimal frequency compensation is impossible [2]. Better solutions are to use a 3x current mirror topology or a zener diode in the differential pair tied between the sources of the N differential pair and the sources of the P differential pair. These circuits adjust the reference current dynamically through the differential pair to minimize g_m deviations when transitioning from the NMOS differential pair to the PMOS one.

The 3x current mirror scheme is employs a 3 time magnification of the current difference between the N and P common mode sensors (refer to figure 13). The N pair common mode sensor creates the current **In** through the two NMOS devices on the far right, and the current **Ip** is produced in the same fashion on the left. A drawback to this method is that it requires the device transconductance parameters of the N and P devices to match. If these parameters do not match,

then the g_m of the differential pair will not be the same when the NMOS input pair is on as when only the PMOS input pair is on. In general, g_m has the following form:

$$g_m = \sqrt{2 \times \mu \times C_{OX} \times \left(\frac{W}{L}\right) \times I_D} = \beta \times \sqrt{I_D}$$

In the 3x current mirror topology case, g_m has the form:

$$g_m = \beta \times \sqrt{I_{DN}} + \beta \times \sqrt{I_{DP}} = \beta \times \left(\sqrt{I_{DN}} + \sqrt{I_{DP}}\right) = \beta \times \left(\sqrt{4I_N - 3I_P} + \sqrt{4I_P - 3I_N}\right)$$

Below is the 3x current mirror topology:

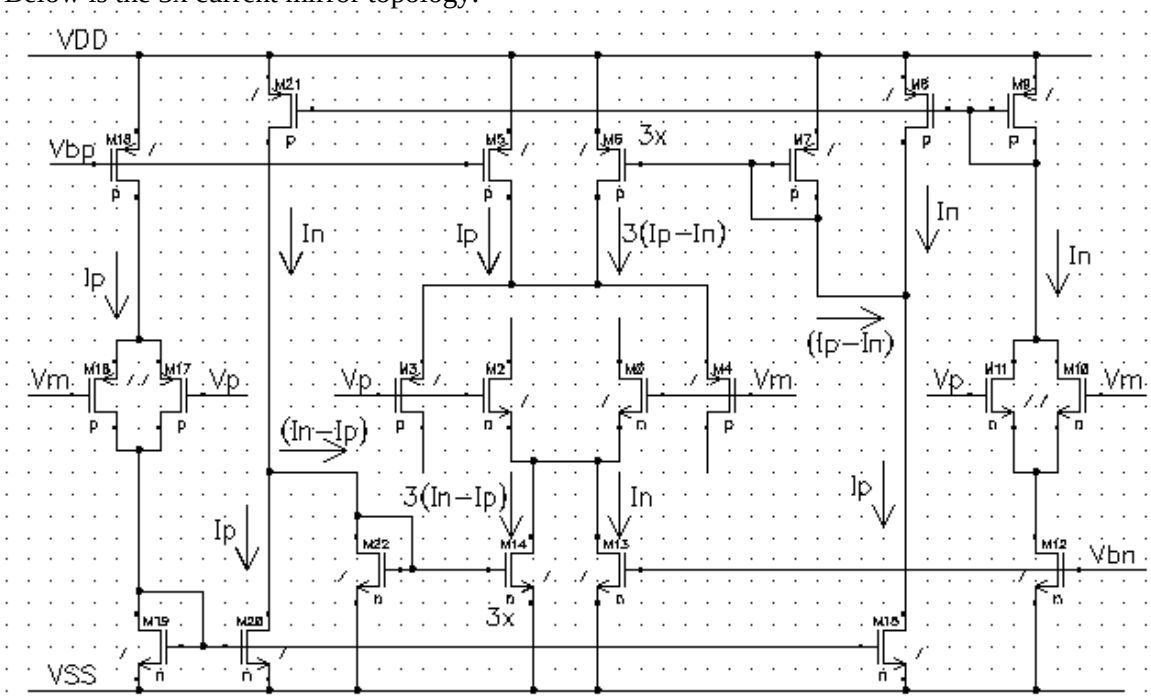


Figure 13: 3x current mirror differential pair topology.

Variations in g_m over the rail to rail range of V_{CM} are due to the $\sqrt{I}$ dependence of the g_m of the differential pair biased in strong inversion [11]. A typical g_m versus V_{CM} curve might look like this:

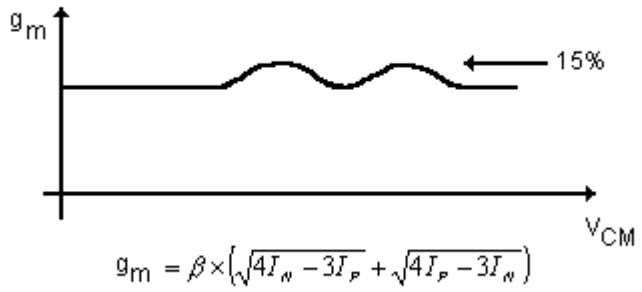


Figure 14: gm over the common mode input range.

Other topologies such as an input stage with a zener diode are capable of a deviation in g_m of only 6%. With such a circuit, zener behavior is mimicked by an arrangement of MOS devices designed to keep the voltage between the N and PMOS differential pair drains constant. This greatly reduces the variation in g_m over the full range of V_{CM}[2].

Switched Capacitor

At voltages of 1V to 2V, switched capacitor is the only technique that can be used to produce good quality analog circuits. Switched capacitor circuits are attractive because it is possible to achieve high filter accuracy with a low distortion. This holds true even as supply voltages decrease because switched capacitor circuits are more susceptible to distortion arising from capacitor non-linearities than decreasing supply voltages (if sufficient opamp gains are maintained) [17]. This is different than other circuits such as g_m-C filters whose operational transconductance amplifiers suffer non-linearities as voltages decrease [18] causing distortion.

Switched capacitor circuits earned their name by switching capacitor terminals between different nodes in a circuit to mimic resistor behavior. These systems are inherently sampled systems. By using switched capacitor building blocks in analog to digital converters, sample and holds can be avoided at the front end. Below are some basic switched capacitor circuits:

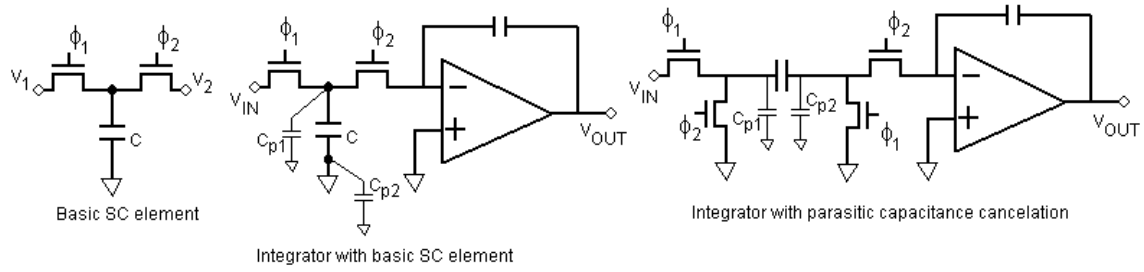


Figure 15: Basic switched capacitor circuits

On the left is the most basic switched capacitor structure. The two switches are controlled by non-overlapping clocks called Φ_1 and Φ_2. First switch one closes and a certain amount of charge defined by $Q = CV_1$ pours into the capacitor. Next, switch two closes and a charge $Q = CV_2$ is transferred. Therefore the total charge transferred can be identified as:

$$\Delta Q = Q_1 - Q_2 = C \cdot V_1 - C \cdot V_2 = C(V_1 - V_2).$$

This means the average current through the device is

$$I_{AVG} = \frac{C(V_1 - V_2)}{T}$$

where T is the period of the clocks. It can be seen from this equation that the voltage to current relationship is not unlike that of a resistor, except here we have:

$$R = \frac{T}{C} = \frac{1}{C \cdot f}$$

In conclusion the "resistance" can be modified through changing the frequency. This is very advantageous since filters whose poles can be moved by changing the clock frequency can be realized.

The first switched capacitor circuit is built with a parasitic sensitive structure; C_{p1} is in parallel with the input capacitor, thereby increasing the equivalent capacitance of C_1 and increasing the amount of charge passed to C_2. The second topology is insensitive to parasitic capacitances since the positive terminal of C_{p2} is connected to ground during Φ_1 and virtual ground during Φ_2. The second capacitance is indeed in parallel with C_1 during Φ_1, but during Φ_2 it is connected to ground, therefore it does not affect the amount of charge passed to C_2.

Accurate switched capacitor circuits can be realized by using differential techniques. Filters aren't the only circuits that can be created by using switched capacitor techniques. Other examples include sample and holds (with or without gain), amplitude modulators, full-wave rectifiers, peak detectors, and oscillators [19].

Switched-Opamp

As voltages drop, it gets harder to realize good switches that can be used in switched capacitor systems. This problem is especially bad once $V_{TN} + V_{TP} + 2\Delta V > V_{DD}$. Possible alternatives include avoiding the gap where the switch conductance is high. This can be done by using a clock voltage multiplier [2], or the novel solution to this problem is described in [9]: to avoid generating high on-chip voltages to control switches or using boot-strap techniques, some of the switches can be removed by switching the opamps. This is accomplished by powering the opamps on an off for the appropriate clock cycles. The technique does have its disadvantages, the main one being a low bandwidth. It takes a relatively long time to switch an opamp on and off compared to an analog switch. Using this technique, the filter below (figure 16) with a THD of –60 dB is reported in a 2.4um process with V_T = +/-0.9V and a 1.5V supply.

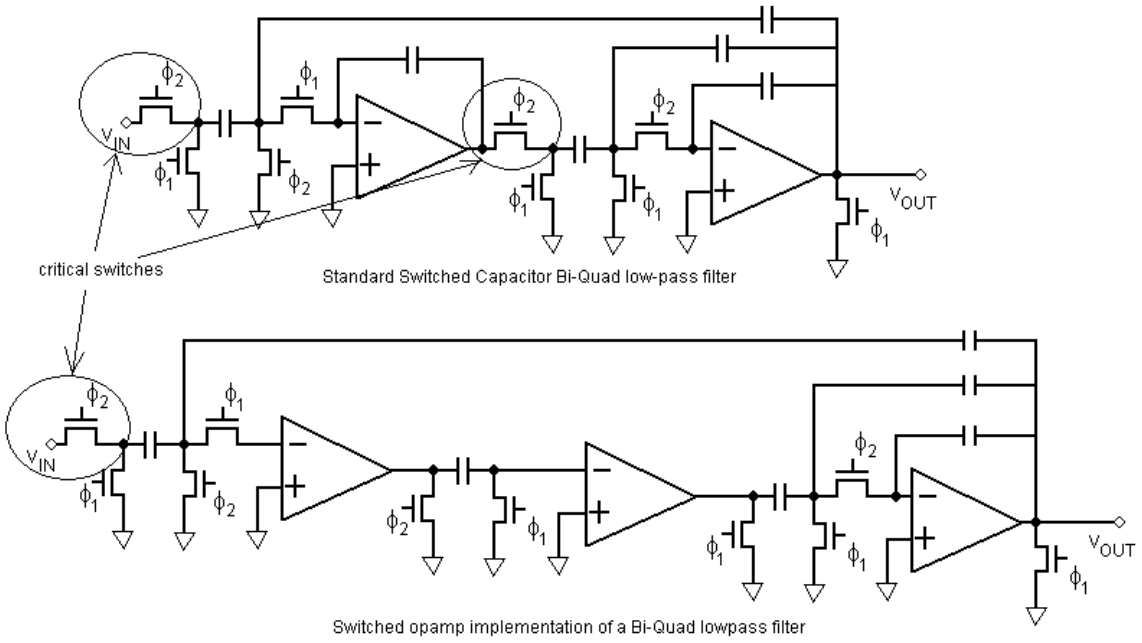


Figure 16: A biquad filter realised using both standard switched capacitor (top) and switched opamp techniques (bottom)

The critical switches in the standard circuit is indicated in the figure, these two are the only two switches in this circuit that have to carry the peak to peak input signal. By using the switched opamp topology, any MOS device that has to switch the entire signal can be eliminated, except for the very first since there is no switched opamp output at that node. The only solution is to replace the first switched capacitor section with a resistor, hearkening back to the continuous-time version of the filter. The use of external components should be minimized, however it might be acceptable in this case. Other circuits that can require external components are reference circuitry, loop filters for PLLs (Phase locked loops), and power pins that might need decoupling.

Sample and Hold

In CMOS processes, sample and hold circuits are most often realized using some variant of the switched capacitor technique. Using the basic switched capacitor element from figure 15 with an analog buffer at the output can create the simplest CMOS sample and hold. If good diodes are available then diode bridge configurations such as the ones described by [6] can be used. A common problem is droop in these types of sample and holds, but this problem can be solved to a first order by operating in a differential fashion. A good example of such a sample and hold can be found in [20].

Charge-Pump Circuits[14]

Charge-pump circuits are used to increase the supply voltage to a level that is useful for analog circuitry. Higher voltages are useful because it makes biasing easier, allows for a larger input range, and switches cannot pass rail to rail signals [1]. Higher voltages are also used in programming non-volatile memories, and in some integrated display drivers.

Some of the problems with charge-pump circuits include an excessive gate overdrive, which can lead to oxide reliability problems in the long-term [1]. Processes designed to run at a low voltage cannot always support larger gate voltages. Therefore, some processes include two types of transistors: the standard high performance type, and a transistor with a thicker gate oxide.

Most charge pumps are based on a circuit proposed by Dickinson [15]. In this circuit, the MOSFETs are wired in a diode configuration, so charge can only flow in one direction. Through the coupling capacitors, the clocks push the charge upwards creating a ΔV at each node equal to:

$$\Delta V = V_{\Phi} \cdot \frac{C}{C + C_S} - \frac{I_O}{f \cdot (C + C_S)}$$

where C is the node capacitance, C_S is the parasitic node capacitance, f is the clock frequency, and I_O is the load current. Refer to figure 17 (below):

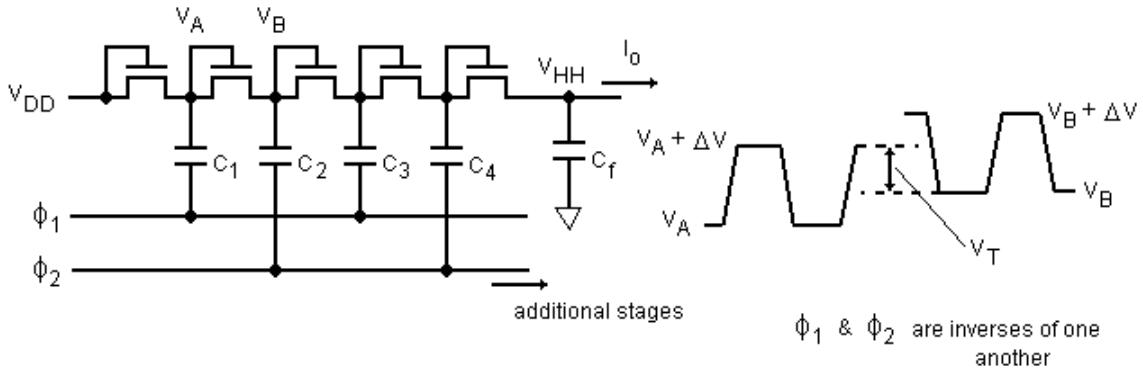


Figure 17: Four stage Dickson charge pump.

This circuit is not perfect since there is a voltage loss of V_T at each stage. The gain of each stage is reduced in low voltage operation since there is less room between V_T and V_{DD}. In this case, ΔV is not much larger than V_T so the body effect can no longer be ignored. This effect is worse at the higher voltage nodes, and the number of stages this circuit can have is limited when the body effect causes V_T to equal ΔV. Floating wells can be used (although they might not be available), however this can result in undesirable substrate currents and the gain in each stage is still reduced by V_T.

Better charge pumps can be attained by using static charge transfer (CTS). These charge pumps do not have their per-stage gains reduced by V_T and can attain higher output voltages. CTS charge pumps use switches to move charge through the stages, thereby eliminating the V_T voltage drop (as seen in Dickson type charge pumps). This effect is achieved by controlling the gate with the voltage of a later stage [15].

MOS Capacitors [10]

It is also important to mention the use of MOS capacitors in low voltage CMOS designs since poly-poly capacitors are often unavailable. In case where processes are optimized for low voltage digital circuits, poly-metal and metal to metal capacitors take up too much space. MOS capacitors can sometimes be used instead of other capacitors which are considered parasitic to digital designers.

A MOSFET capacitor is a transistor that has its source and drain connected to ground, hence the gate oxide is the capacitor dielectric, and the gate is the positive terminal to the capacitor. MOS capacitors have two major advantages to other capacitors available in CMOS. The first is that they are formed with a thin layer of gate oxide (measured as t_{ox} in SPICE), and since capacity is inversely proportional to the distance between the plates, a larger capacitance per unit area can be achieved. The second major advantage is that there is a low parasitic capacitance since the capacitor is not floating above the substrate, hence there is no bottom plate to substrate parasitic capacitance. Another advantage is that these capacitors have better matching since there are tighter tolerances associated with the construction of transistors, the main one being the dielectric material thickness is well controlled. Figure 18 below shows the four types of MOS transistors and a floating capacitor:

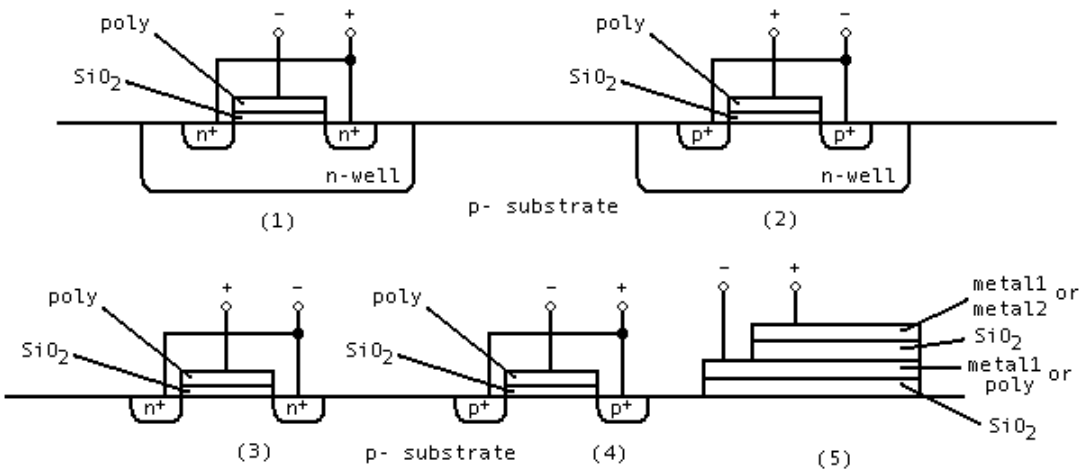


Figure 18: Examples of capacitors in MOS.

The SiO_2 is the thinnest between the gate layer and substrate; SiO_2 between other layers such as metal one and poly are much thicker to reduce "parasitic" capacitances. From device (5) it can be seen that there is a parasitic capacitor between the minus terminal and the substrate. There will also be a parasitic capacitance between the upper plate and the substrate because at some point the upper plate will hang off the lower plate. Great care must be taken in all of these devices to ensure the silicon under and around them is biased to the correct potential to avoid forward biasing of parasitic diodes that are formed. The best MOS capacitor is the first one shown in figure 18 because it has the least dependence of capacitance on gate voltage. For these devices, this is the major drawback – the gate voltage has a larger effect on capacitance. Figure 19 below illustrates this effect:

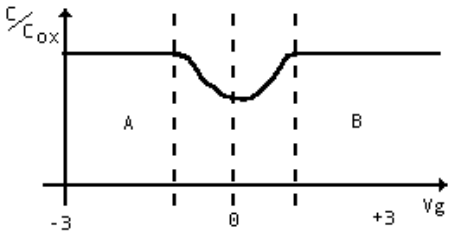


Figure 19: MOS capacity versus gate voltage.

Obviously these are not ideal capacitors, but they can still be used if they are operated in A – the Strong Inversion region, or B – the Accumulation region. If designed carefully, these capacitors can be used inside switched capacitor circuits, but input and output capacitors still need to be linear. In low voltage designs, it might not be possible to keep common mode voltages high enough to keep them in their linear regions. Even if they are not always operated in these two regions, MOS capacitors can still be useful where the application is not sensitive to capacitor accuracy. Such applications include compensation for opamps, in power on reset circuitry, or as local bypass capacitors for circuits sensitive to power supply noise.

Conclusion

Analog circuit design is certainly not as easy as digital to scale down to the lower voltages of the most current processes. In some cases it is impossible to run analog circuits at low voltages without process modifications such as devices with lower threshold voltages. Processes designed to accommodate mixed signal circuits (both analog and digital) add extra steps to create transistors that can operate at higher voltages. Unfortunately this compromise increases the per-unit cost of microchips.

At this point in time, using current low voltage techniques, it is very difficult to realize high performance analog circuits. The benefits of low voltage analog design are great from an economical standpoint. If we can eliminate the extra processing steps required by analog circuits, the process becomes cheaper by reducing the effort spent on modeling and designing a process with multiple types of transistors.

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