Imre Knausz

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OBJECTIVE A position in analog or mixed-signal IC design, or alternatively, a demanding circuit and architecture design position with the opportunity to learn and use my creativity.

EDUCATION

Rochester Institute of Technology, Rochester, NY, MS in Electrical Engineering 2005

Rensselaer Polytechnic Institute, Troy, NY, BS in Electrical Engineering 1999

TECHNICAL EXPERIENCE

Synaptics, Inc., Pittsford, NY, headquarters in Santa Clara, CA 2/2009-present

Analog/Mixed Signal Design Manager

- Analog design manager on a small format LCD driver design team that requires working on a large multi-disciplinary team including an existing design team in California. Manage 4 direct reports.
- Working on merging two existing designs from two companies into one product which requires understanding architectures of two very different integrated circuits (IC). This has required frequent travel and good communication to come up the learning curve on new products and circuits. Driving integration of the two architectures and verification environments. Verification methodologies are also being merged and result in adequate coverage.
- Presented a two day technical seminar to train the California design team on high voltage circuit techniques in low voltage processes.
- Designing Electrostatic Discharge (ESD) circuits for the new product through evaluation of previous products and new product requirements.
- Evaluating several foundries' capabilities to find an optimal semiconductor manufacturing process for display driver circuits. This requires in depth device physics knowledge in order to push process limits using standard processing practices to gain a competitive edge.

National Semiconductor, Pittsford, NY 8/2001-1/2009

Senior Analog/Mixed Signal IC Designer, Analog Team Leader

- Analog team leader on a small format LCD driver design that required working on a large multi-disciplinary team and directing 6 analog circuit designers with several in remote locations. In addition to porting to a deep submicron process, several features were added including increasing drive capability to WVGA resolutions (480x850 pixels) and outputting negative as well as positive drive voltages (10V output in a 5V process). Redesigned much of the architecture to enable new features and to take advantage of the new process. Managed analog design tasks for the team such as project schedules, documentation, regular status updates, and deciding which engineers were best suited to certain design tasks. Developed chip architecture and feature implementations with the design management team.
- Mixed signal design engineer for an advanced LCD high resolution display driver. Created novel architectures for displays up to HVGA in resolution (320x480 pixels). Designed opamps and D/A circuits that solved the challenge of driving larger loads while maintaining low power. Provided technical support in every step of the silicon validation and production test phases including reviewing test results. Successfully went to production with major cell phone manufacturers, over 10 million units delivered.
- Designed various circuit blocks such as successive approximation ADCs, oscillator, current mode DACs, gamma DACs, high voltage level shifters in a low voltage process, low voltage level shifters, I/O cells, and ESD protection schemes.
- Hands on experience in lab validation using probe stations, various test equipment and LabView with GPIB control of instruments. Worked extensively with local test engineer to write and debug analog production tests. Several trips to Taiwan were required to successfully debug production analog tests. Identified design for test issues with test engineer and designed internal circuitry to facilitate efficient testing.

- Performed chip level verification using SpectreVerilog and AMS mixed mode simulations and transistor level simulations on multimillion transistor system on a chip designs. Experienced with high capacity table model simulators. Wrote high level verilog models for several analog blocks. All blocks in the system had verilog models to allow several configurations of analog and digital modeling to enable system level verification with reasonable run times.
- Designed ambient light sensor to enable control of the LCD backlight according to lighting conditions to save power. Work on this block included writing verilog RTL to control the ADC.
- Designed a 528 channel non-linear Digital to Analog Converter to drive color small format liquid crystal displays (176x240 pixels). The DAC has a 6-bit resolution and drives red, green and blue pixels for an effective full color resolution of 18-bits. DAC design also called for the design of an ultra low power rail to rail operational amplifier. Heavily involved in floor-planning and directed layout to control process variation induced circuit inaccuracies. Assisted in architectural decisions.
- Served in a mentor role over the past two years for engineering co-op students.

LSI Logic, Fairport, NY 1/2000-8/2001

ASIC Design Engineer

Analog and Digital ASIC design experience. Performed Verilog modeling and layout of digital primitives. Designed, simulated, and created the layouts for a Flash A/D converter, Power On Reset circuitry, Line Rate Clamp and other circuits. Project leader for a dual 10-bit current mode DAC IC that went through the entire ASIC flow including:

- IP reuse and verification - Reused a 10-bit DAC and bandgap circuit from company IP library. Created top level schematic including design of glue logic. Simulated entire IC over worst voltage, temperature, and process corners.
- Layout - Created floor plan based on two existing cells, glue logic, and customer requirements. Supervised two mask designers through the entire layout phase being mindful of parasitic loading at DAC outputs, parasitic resistances causing on-chip voltage drops, and symmetry issues.
- Bonding and package selection - Selected package based on acceptable parasitic capacitance and pinout requirements. Created bonding diagram based on floor plan and customer requirements.
- Complete test - Setup up laboratory for testing ICs. Designed evaluation board used for interfacing ICs to the test equipment. Tested DACs for linearity (Gain, Offset, INL and DNL), dynamic performance (SINAD, SNR, SDR) and bandgap performance. Automated entire test suite through LabView with lab instruments connected to a PC through GPIB and TCP/IP. Created a system for storing data when it is collected and parsing through the data. Wrote characterization reports.

Plug Power, L.L.C., Latham, NY 1/1999-12/1999

Intern Electrical Engineer

Designed circuits and programmed microcontrollers for embedded control applications. Aided in the hardware design of a modular microprocessor controlled differential voltage scanner card that communicated over an isolated multi-drop network; performed all software design.

PATENTS AND PUBLICATIONS

US07362173 - 4/22/2008: *System and Method for Providing Slew Rate Enhancement for Two Stage CMOS Amplifiers* (http://www.knausz.com/7362173-cmos-amplifiers)

US07504979 - 8/21/2009: *System and method for providing an ultra low power scalable digital-to-analog converter (DAC) architecture* (http://www.knausz.com/7504979-low-power-dac)

International Solid State Circuits Conference, San Francisco, CA 2/7/2006

A 250µW 0.042mm^2 2MS/s 9b DAC for Liquid Crystal Display Drivers

The architecture and design methods are presented for implementing N-bit DACs optimized for small-format LCD column drivers. Individual 9b DACs in a 12-channel display system occupy a die area of 0.042mm^2. This represents a composite DAC performance of better than 0.60pJ/b/mm^2. (Presentation and published paper available upon request)

Journal of Solid State Circuits 9/2009

A Low Power, Scalable, DAC Architecture for Liquid Crystal Display Drivers

This paper describes a low-power, area efficient, scalable, digital-analog conversion (DAC) integrated circuit architecture. A 12 channel, 9-bit DAC driver based on this architecture, implemented in 0.5 µm CMOS technology and suitable for 1/4 VGA resolution displays, exhibited a 2 MSPS conversion rate and 252 µW power dissipation per channel. (Published paper available upon request)

COMPUTER EXPERIENCE

Languages:

Verilog, VerilogA, VHDL, C & C++, Perl, UNIX shell, Visual Basic, HTML, PHP, Pascal, PIC Assembly

Software:

UNIX (Solaris, Linux), Windows, Cadence Design Suite, Mentor DA & IC, LabView, Maple, Matlab, PSpice, OrCAD, Microsoft Office (including Visual Basic macros), Drupal, Adobe PhotoShop

LANGUAGES Fluent in English and Hungarian

ACTIVITIES / HOBBIES Vacuum tube amplifier design and construction, guitar, running, ice hockey

CITIZENSHIP United States

Reference available upon request.